IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A silicon wafer wherein stacking fault nuclei are distributed throughout the entire in-plane direction, and a density of said stacking fault nuclei is set to a range of between $0.5x10^{8}cm^{-3}$ and $1x10^{11}cm^{-3}$.

2. (Currently Amended) A silicon wafer according to claim 1, which is cut from an ingot formed from a perfect region wherein interstitial silicon-type point defect agglomerates and vacancy-type point defect agglomerates are ~~practically~~ substantially non-existent.

3. (Original) A silicon wafer according to claim 1, which is cut from an ingot formed from a region wherein vacancy-type point defects are dominant.

4. (Currently Amended) A manufacturing method of a silicon wafer ~~wherein~~ , comprising pulling an ingot ~~pulled~~ from a silicon melt in a crucible in accordance with the Czochralski method , and slicing the ingot ~~is sliced~~ to manufacture the silicon wafer according to claim 1,

wherein said ingot is pulled such that a ratio V/G of, a rate V at which the ingot is pulled, and a temperature gradient G of the ingot in the vertical direction in the vicinity of an interface between the silicon melt in the crucible and the ingot, is between $0.20mm^{2}/°C \cdot minute$ and $0.25mm^{2}/°C \cdot minute$.

5. (Currently Amended) A manufacturing method of a silicon wafer ~~wherein~~ , comprising pulling an ingot ~~pulled~~ from a silicon melt in a crucible in accordance with the

Czochralski method , and slicing the ingot ~~is sliced~~ to manufacture the silicon wafer according to claim 1,

wherein nitrogen is added while pulling said ingot, to set an internal nitrogen concentration within a range of between $5x10^{14}cm^{-3}$ and $5x10^{15}cm^{-3}$.

6. (Currently Amended) A manufacturing method of a silicon wafer which manufactures the silicon wafer according to claim 1, comprising:

[[a]] vacancy heat ~~treatment step~~ treating for forming new vacancies in the interior by means of a heat treatment of said silicon wafer in an atmosphere gas containing nitrogen; and

~~an~~ SF nuclei heat ~~treatment step~~ treating which agglomerates interstitial silicon released during precipitation of oxygen from vacancies injected by said vacancy heat treatment step, to form stacking fault nuclei,

and a temperature in said SF nuclei heat ~~treatment step~~ treating is above 1100°C, and is increased at a rate of not more than 10°C/minute.

7. (Currently Amended) A manufacturing method of a silicon wafer according to claim 6, wherein an oxide film on the surface of said silicon wafer is ~~previously~~ removed[[,]] prior to said vacancy heat ~~treatment step~~ treating.

8. (Currently Amended) A manufacturing method of a silicon wafer according to claim 6, wherein during said vacancy heat ~~treatment step~~ treating, purging is conducted to remove oxygen from the atmosphere gas surrounding said silicon wafer, and said silicon wafer is quenched after said vacancy heat ~~treatment step~~ treating.

9. (Currently Amended) A manufacturing method of a silicon wafer comprising ~~a step of~~ heat treating to the silicon wafer according to ~~one of claims 1 and 2~~ claim 1, ~~or, to the silicon wafer manufactured by the manufacturing method of a silicon wafer according to any one of claims 3 to 8,~~ to form at least a defect-free layer on the surface of said silicon wafer.

10. (Currently Amended) A silicon wafer manufactured by the ~~manufacturing~~ method of ~~a silicon wafer according to~~ claim 9.

11. (New) A manufacturing method of a silicon wafer comprising heat treating the silicon wafer according to claim 2, to form at least a defect-free layer on the surface of said silicon wafer.

12. (New) A silicon wafer manufactured by the method of claim 11.

13. (New) A manufacturing method of a silicon wafer comprising heat treating the silicon wafer manufactured by the method of claim 3, to form at least a defect-free layer on the surface of said silicon wafer.

14. (New) A silicon wafer manufactured by the method of claim 13.

15. (New) A manufacturing method of a silicon wafer comprising heat treating the silicon wafer manufactured by the method of claim 4, to form at least a defect-free layer on the surface of said silicon wafer.

16. (New) A silicon wafer manufactured by the method of claim 15.

17. (New) A manufacturing method of a silicon wafer comprising heat treating the silicon wafer manufactured by the method of claim 5, to form at least a defect-free layer on the surface of said silicon wafer.

18. (New) A silicon wafer manufactured by the method of claim 17.

19. (New) A manufacturing method of a silicon wafer comprising heat treating the silicon wafer manufactured by the method of claim 6, to form at least a defect-free layer on the surface of said silicon wafer.

20. (New) A silicon wafer manufactured by the method of claim 19.

21. (New) A manufacturing method of a silicon wafer comprising heat treating the silicon wafer manufactured by the method of claim 7, to form at least a defect-free layer on the surface of said silicon wafer.

22. (New) A silicon wafer manufactured by the method of claim 21.

23. (New) A manufacturing method of a silicon wafer comprising heat treating the silicon wafer manufactured by the method of claim 8, to form at least a defect-free layer on the surface of said silicon wafer.

24. (New) A silicon wafer manufactured by the method of claim 23.